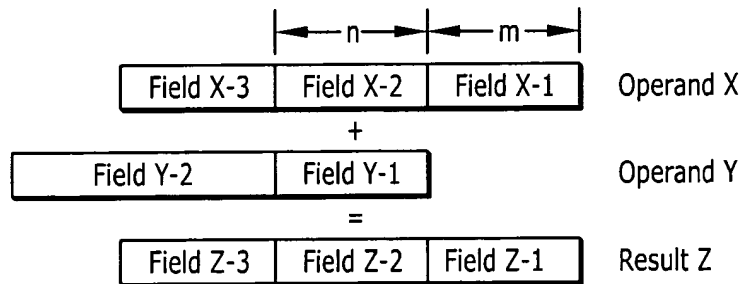
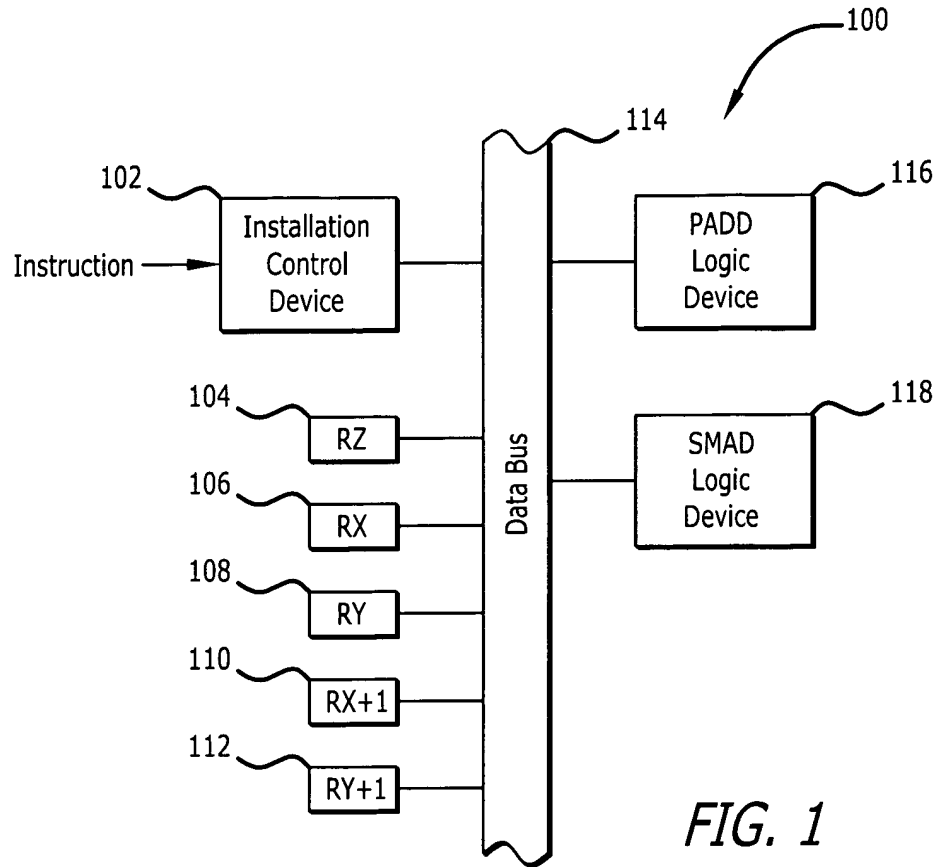




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Instruction Description

- PADD

Syntax: PADD [-C][-M] RZ, RX, RY
PADD -I[-C][-M] RZ, RX, <UI8 :immediate>
PADD -N[-C][-M] RZ, RX, RY, <UI5 : start>, <UI5 : stop>
PADD -N-I[-C][-M] RZ, RX, <UI8 : immediate>, <UI5 : start>

RX, RY are the source data registers
RZ is the destination register
<UI8 : immediate> specifies the value of an immediate operand
<UI5 : start> specifies start of bit field to be modified
<UI5 : stop> specifies end of bit field to be modified
-C indicates addition with carry in
-M indicates addition modulo $2^n - 1$
-N indicates that addition affects only a bit field
-I indicates that second operand is supplied as an immediate value

FIG. 2A

250

Option Used	Operation
PADD RZ, RX, RY	$RZ = RX + RY$
PADD -C RZ, RX, RY	$RZ = RX + RY + Cin$
PADD -I RZ, RX, <UI18: Immediate>	$RZ = RX + <immediate>$
PADD -N RZ, RX, RY, <UI5: Start>, <UI5: stop>	$RZ = \{ RX[start:stop], (RX[stop:start] + RY[length] + RX[start:0]) \text{ modulo } 2^{length} \}$ <p>Where length = stop - start + 1</p>
PADD -M RZ, RX, RY	$RZ = (RX + RY) \text{ modulo } 2^{n-1}$
PADD -N -I RZ, RX, <UI8: immediate>, <UI5: start>	$RZ = \{ (RX[31:start], + immediate[31-start:0]) \text{ modulo } 2^{31-start+1}, RX[start:0] \}$ <p>In this case, a stop is assumed to be 31.</p>

FIG. 2B

300

SMAD

Syntax: SMAD [-A] [-M] RZ, RX, RY, <UI2: Length>, <UI2: Num Ops>

RZ is the destination register

RX and RY are source data registers

-A option is used to accumulate results where RZ is used as the accumulator

-M option results in a modulo $2^n - 1$ addition

<UI2: Length> indicates the data widths

- 0: 8 bit operands, where each register is assumed to contain 4 8-bit operands
- 1: 16 bit operands, where each register is assumed to contain 2 16-bit operands
- 2: 32 bit operands
- 3: unused

<UI2: Num Ops> indicates the number of operands to be used in the addition

- 0: 2 source operands RX and RY
- 1: 3 source operands RX, RX+1 and RY
- 2: 3 source operands RX, RY and RY+1
- 3: 4 source operands RX, RY, RX+1 and RY+1

FIG. 3A

350

Option Used	Operation
SMAD RZ, RX, RY, 2, 0	
SMAD -A RZ, RX, RY, 2, 0	$RZ = RZ + RX + RY$
SMAD RZ, RX, RY, 2, 3	$RZ = RX + RY + (RX+1) + (RY+1)$
SMAD RZ, RX, RY, 0, 0	$RZ = RX[7:0] + RX[15:8] + RX[23:16] + RX[31:24] +$ $RY[7:0] + RY[15:8] + RY[23:16] + RY[31:24]$
SMAD -M RZ, RX, RY, 2, 0	$RZ = (RX + RY) \text{ modulo } 2^n - 1$
SMAD -A -M RZ, RX, RY, 2, 0	$RZ = (RZ + RX + RY) \text{ modulo } 2^n - 1$

FIG. 3B

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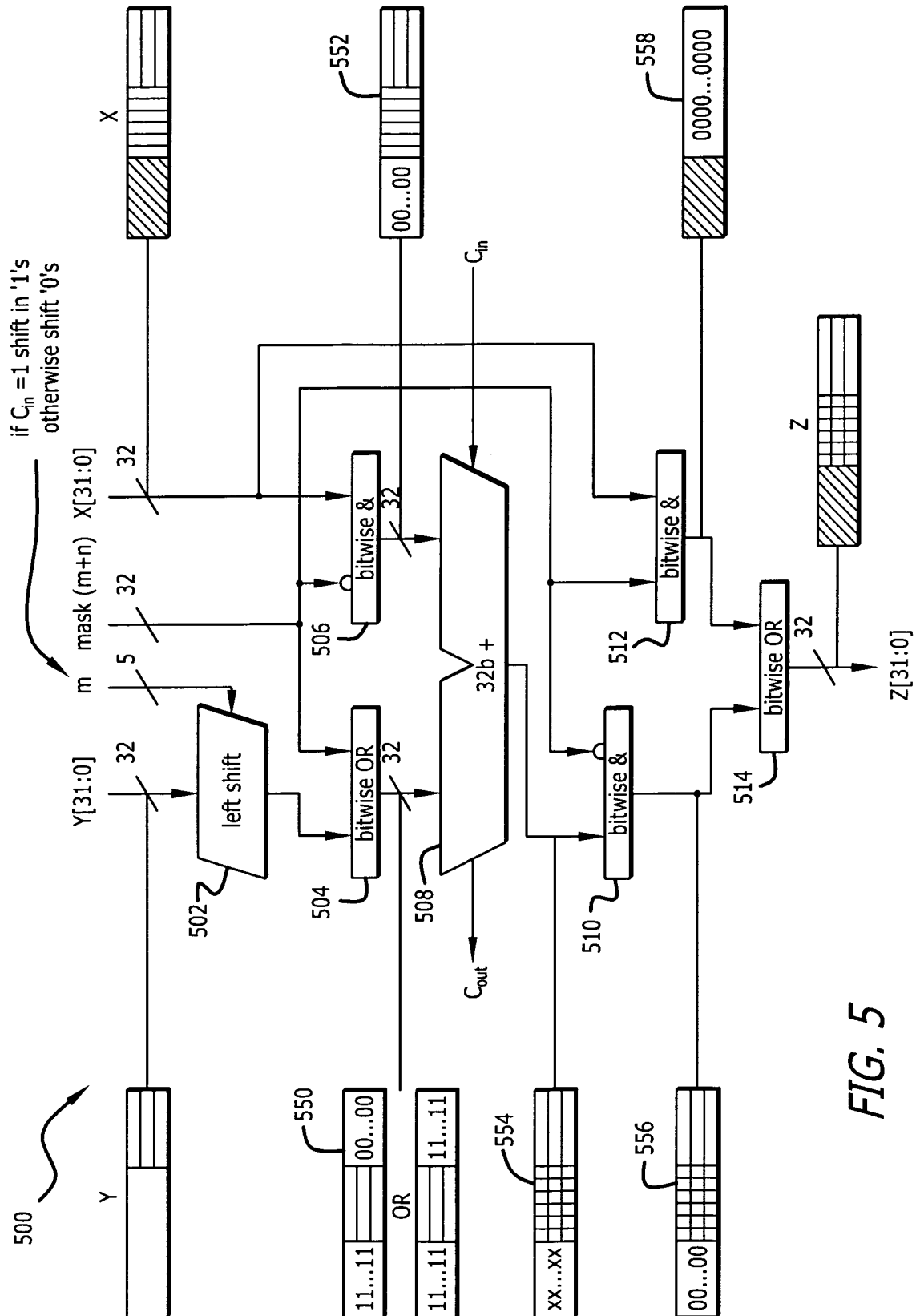


FIG. 5

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$m + n$	mask (32b)	$\overline{\text{mask}} (32b)$
0: 00000	1111...1110	0000...0001
1: 00001	1111...1100	0000...0011
2: 00010	1111...1000	0000...0111
⋮	⋮	⋮
30: 1_1110	1000...0000	0111...1111
31: 1_1111	0000...0000	1111...1111

FIG. 6

Carry bits of special consideration in "32-b CSA"			
carry bit	output from	input to	not propagated for modulo 2^n addition, $n=?$
c[8]	702-7	704-8	8
co_8	702-7	702-8	8
c[16]	702-15	704-0	8, 16
co_16	702-15	702-16	8, 16
c[24]	702-23	704-8	8
co_24	702-23	702-24	8
c[32]	702-31	708	8, 16, 32
co_32	702-31	702-0	8, 16, 32

FIG. 11

Carry bits of special consideration in "16-b CSA"			
carry bit	output from	input to	not propagated for modulo 2^n addition, $n=?$ ($n = 32$ not applicable)
c[8]	704-7	706-0	8
co1_8	704-7	704-8	8
c1[16]	704-15	704-0	8, 16
co1_16	704-15	704-0	8, 16

FIG. 12

Carry bits of special consideration in "8-b CSA"			
carry bit	output from	input to	not propagated for modulo 2^n addition, $n=?$ ($n = 32, 16$ not applicable)
c2[8]	706-7	706-0	8
co2_8	706-7	706-0	8

FIG. 13

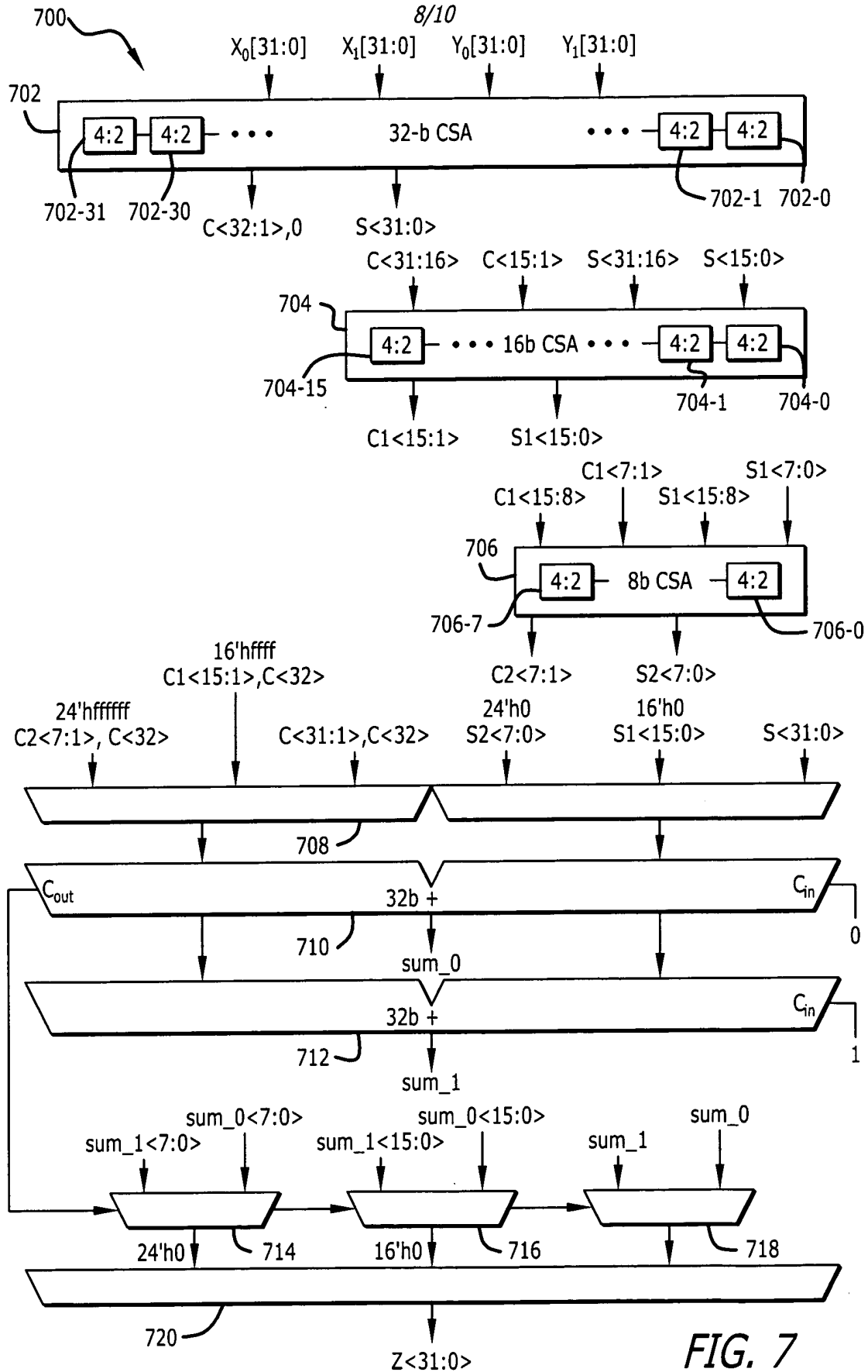
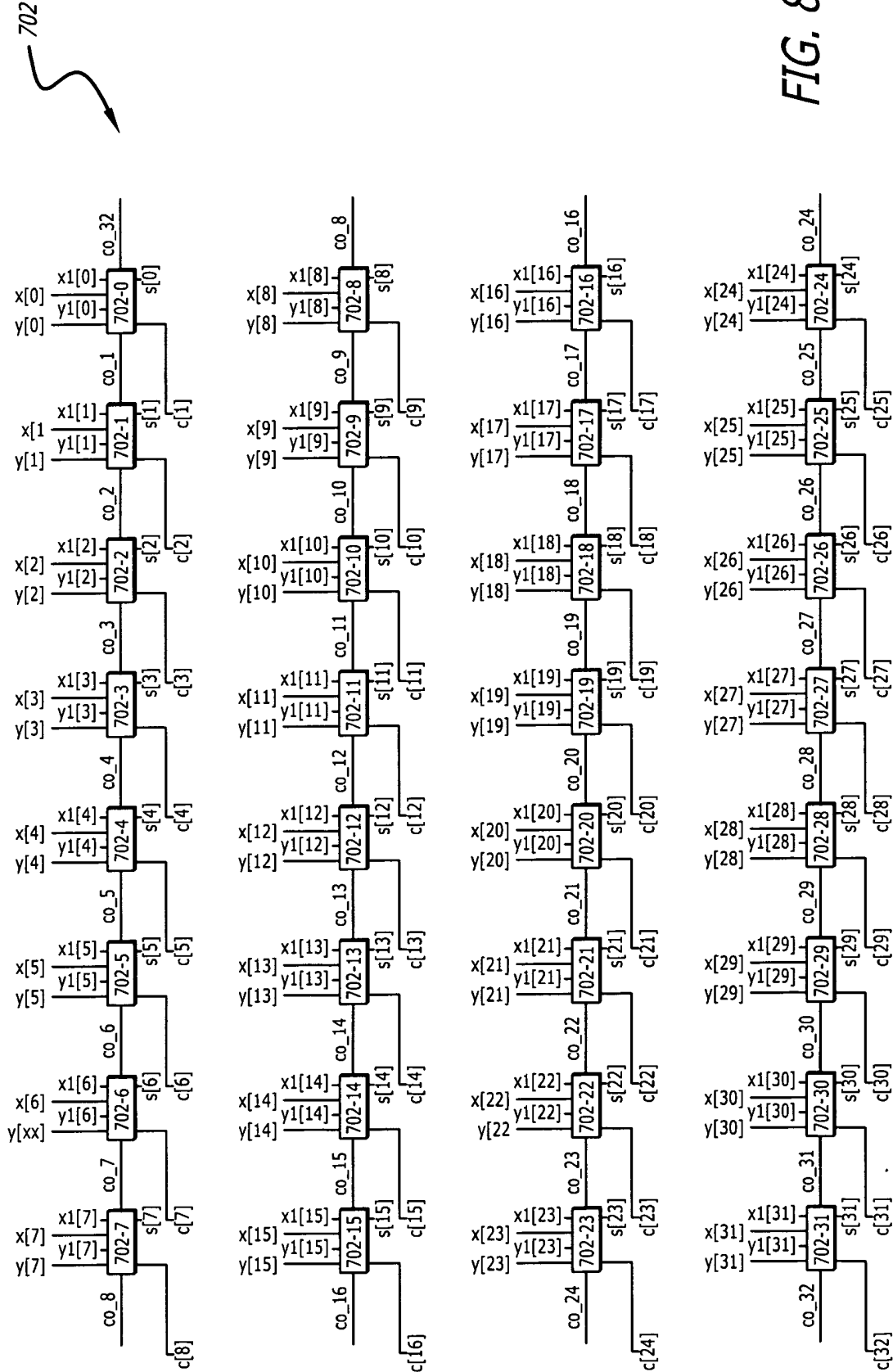


FIG. 7



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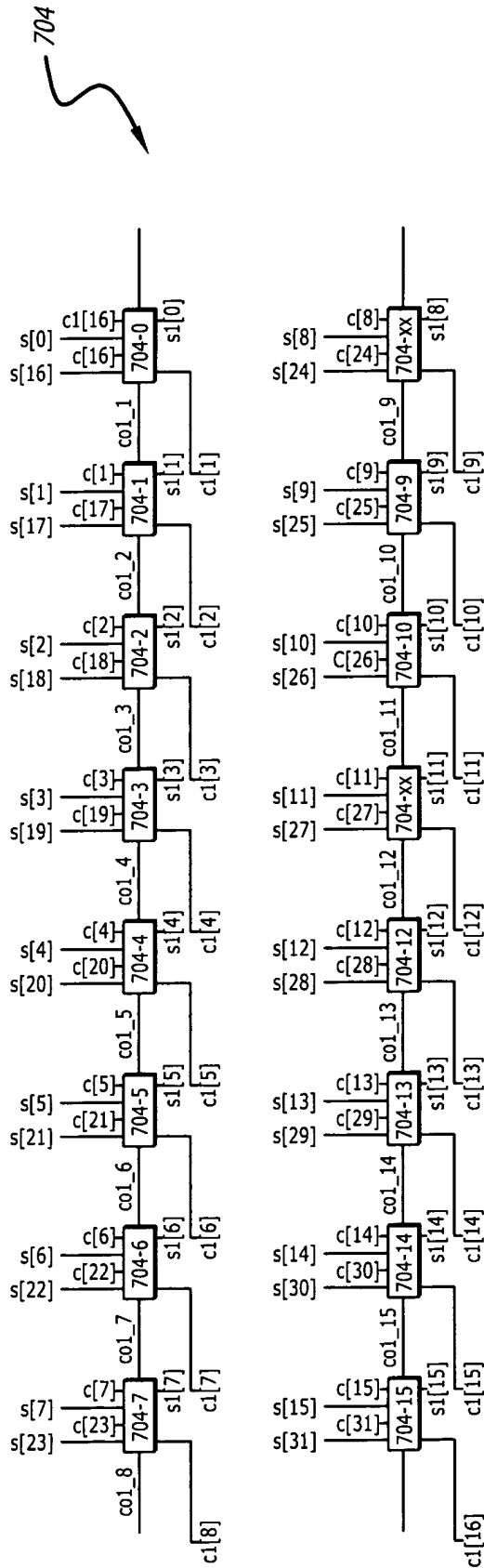


FIG. 9

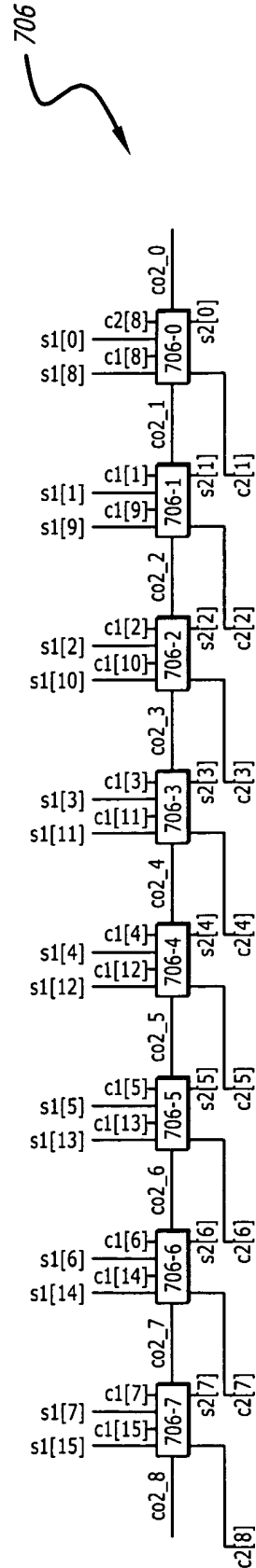


FIG. 10